Options for Hardening FinFETS with Flowable Oxide Between Fins

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Abstract: *A methodology using radiation-induced charge measurements by CV techniques on blanket oxides is shown to aid in the choice of process options for hardening FinFETs. Net positive charge in flowable oxides was reduced by 50 % using a simple non-intrusive process change. This process translates into a 10x reduction in radiation induced offstate current for nFinFETs.*

Keywords: FinFETs; Radiation

Introduction

Bulk silicon 14 nm nFinFETs have been shown to be TID radiation sensitive due to significant increases in offstate current.[1,2] Radiation-induced net positive charge buildup in the oxide between fins causes leakage current in lightly doped subfin neck regions. Fig. 1 shows the location of the subfin leakage path caused by radiation-induced net positive charge build up in the shallow trench isolation (STI) oxide fill region.

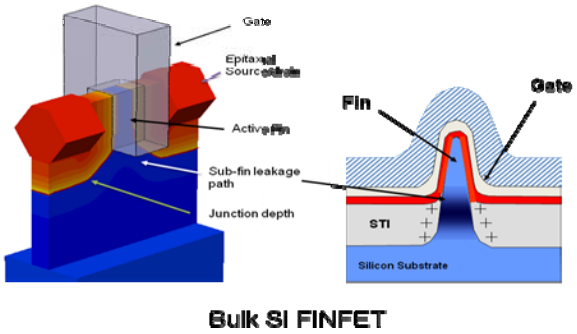

Figure 1. Fin structure [3] showing radiation-induced net positive charge build up in STI fin fill oxide regions causing leakage paths in the sub-fin region of a bulk silicon nFinFET.

FinFET scaling requires reduced fin pitch with improved oxide fill. At the 14 nm node a typical fin pitch of 42 nm is used. Flowable oxide has been introduced to replace HARP (high aspect ratio process) oxide to provide scalable, defect free, high yield oxide fill between fins. A plasma enhanced CVD flowable process using trisilylamine ($:N(SiH_3)_3$) is now being considered for FinFET oxide fill.

Approach

We determined the TID radiation hardness of flowable oxide versus flowable oxide post-deposition heat treatment (process A and process B) using capacitance-voltage (CV) techniques on blanket 48 nm thick oxide films. Flowable oxides were deposited at 65°C, cured in ozone, followed by heat treatments A and B. See Fig. 2 for pre- and post- 1 Mrad CV curves for the two conditions. Fig. 3 shows flat-band voltage shifts taken from CV curves versus X-ray dose indicating the 50% reduction in net positive charge for the flowable oxide with process A compared to process B.

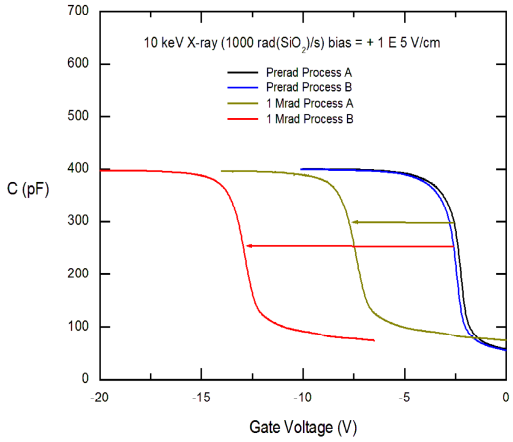

Figure 2. CV curves pre-and post-1 Mrad (SiO_2) X- ray irradiation for flowable oxides with two different post-deposition heat treatments, A and B.

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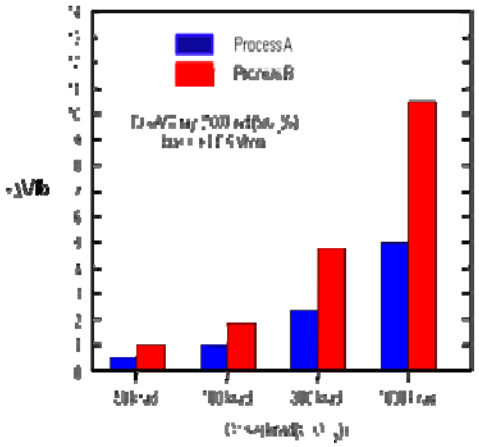

Figure 3. Flat band voltage shifts from CV curves versus total X-ray dose for flowable oxides A and B. The appropriate electrical bias was determined using TCAD simulations.

Flowable oxide types A and B were used in the fabrication of FinFETs. Current/voltage plots are shown in Fig.4 and Fig. 5. Fig. 4 shows that radiation hardening is provided up to a dose of 1 Mrad(SiO_2). No significant increases are observed in offstate current for FinFETs fabricated using type A flowable oxide.

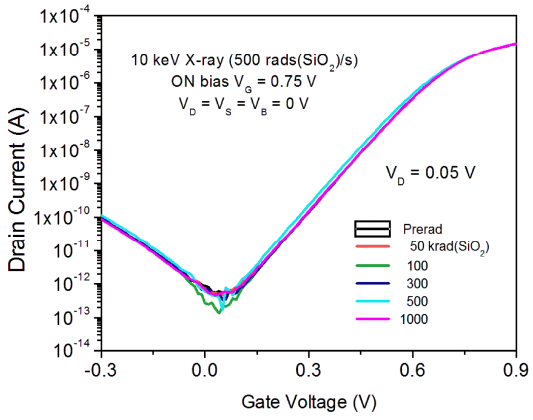

Figure 4. Current –Voltage curves versus 10 keV X-ray dose (517 rad(SiO_2)/s) for bulk nFinFETs with flowable oxides type A. ON bias was applied during irradiation.

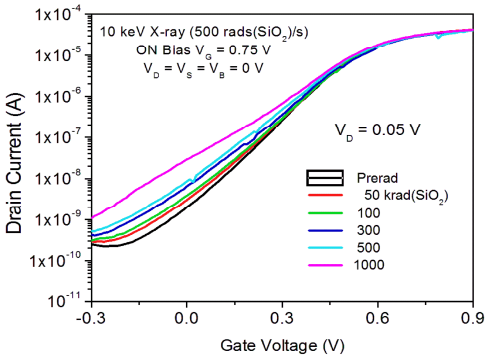

Figure 5. Current –Voltage curves versus 10 keV X-ray dose (517 rad(SiO_2)/s) for bulk nFinFETs with flowable oxide B. ON bias was applied during irradiation.

Conclusion

A new CMOS TID radiation vulnerability has been identified with no obvious hardening-by-design remedy, thus hardening by process is needed. Using the methodology of CV measurements on inexpensive experimental blanket oxides we have determined options for hardening FinFETs without expensive building and testing developmental FinFETs. For example choosing experimental process option A over process B yields a megarad hard FinFET.

References

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